

**Pan-STARRS PS1 STARGRASP Controller**  
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## ABSTRACT

The requirements for rapid readout and low noise combined with the unprecedented number of pixels in the Pan-STARRS camera (~1.4 Gigapixels) poses a challenge for the design of the readout and signal chain electronics. This paper presents the hardware and software design for the Pan-STARRS Scalar Topology Architecture of Redundant Gigabit Readout Array Signal Processors (STARGRASP) controller. Compared to other controllers, the current design also yields a significant reduction in physical size and number of required PCBs with a corresponding reduction in power consumption. Over the past two years, Pan-STARRS controller development has been rapid with the current STARGRASP performance meeting requirements.

## INTRODUCTION

The requirements imposed on the array controller for the PanSTARRS Orthogonal Transfer Array (OTA)<sup>1</sup> in an 8x8 mosaic presents a formidable challenge to any existing design. Despite the presence of an ongoing array controller development program at the Institute for Astronomy, a completely new effort was undertaken to produce a next generation design that could scale up to the needs of a gigapixel focal plane instrument. The team that was assembled to produce this design consisted of 2 scientists, 3 hardware/firmware engineers and 2 software engineers each with specific expertise and experience in critical areas.

## DEVELOPMENT AND INFRASTRUCTURE PLAN

A multiphase plan has been developed to produce the STARGRASP array controller. A distinct infrastructure and prototype phase was identified as critical for success and the Institute for Astronomy has acquired new CAD development tools, Ball Grid Array (BGA) integrated circuit package rework and inspection capability, clean room, and a wire bonder. The BGA rework and inspection tools were especially important because the small form factor requirements for the controller required the use of BGA packages. Optical and X-ray BGA inspection microscopes have already proved valuable in troubleshooting. The prototype phase has been successfully completed, resulting in a electronics board set that is capable of running an individual OTA.

## REQUIREMENTS

### Modes of Operation

The OTA will be operated in a sequence of different modes of clocking and readout to accomplish the overall goal of a corrected science image.<sup>2</sup> The OTA design incorporates specific circuitry that will need to be serviced by the controller electronics to accomplish these modes.

Mode Name	Description	OTA operation	Controller Function Required
Idle	No integration, no guide	Resets?	Reset OTAs?
Shutter Control Mode	No integration, no guide		

Guide Star Acquisition mode	~1 sec Integration ~0.5 sec Readout for ~ 5 guide objects in 5 cells per OTA	Integrate Address cells Clock out	Reset, Integrate timing, Readout, Transport data to Pixelserver computer, Pixelserver computer determines centroids and corresponding clocking patterns for image correction.
Combined Guide and Integration Mode	Fast clocking and readout of Guide cells	Integrate Address cells Clock out	
Low Noise Readout Mode	(Closed shutter) readout of science image	Integrate Address cells Clock out	

The typical sequenced readout of an OTA would be:

Sequenced readout :

Open Shutter

Acquire

~1 sec integration, readout ~0.5sec

Pixelserver determines ~5 guide objects in 5 cells per OTA

Guide + Integration

~5 guide cell subarray readout at 10-30Hz (<100Hz)

Pixelserver centroids and determines guide subarray position

Pixelserver also computes OT parallel shift patterns for remaining cell

Expected Itimes Nominal 10s of seconds

Max ~1000sec

Min ~shutter speed/setup

Apply OT parallel shift clocks (~10usec each)

Delay ~50msec

Close shutter and Readout ~2sec

### Full Camera operation

- Synchronized clocking to <30nsec.
- Heat dissipation from controller system should not impact seeing.
- System will need active cooling.
- System goal of < 400Watts (On Telescope, per Gigapixel Camera).
- Noise floor 1 LSB, less than 1e-.
- OTA crosstalk must be less than noise floor

### OTA Input and Control

- Sequenced readout
- guide rates 10-30Hz
- Nominal guide patch
  - @ 0.3 arcsec/pixel 10 arcsec patch = ~32 X 32 pixels, 10msec/1024 pixels = 9.77 usec/pixel max speed clock+signal condition+ADC+buffer
- Centroid and shift calculation time + Change clock patterns, latency goal = 2msec goal
- Clocking pattern time resolution ~10nsec

### OTA Output

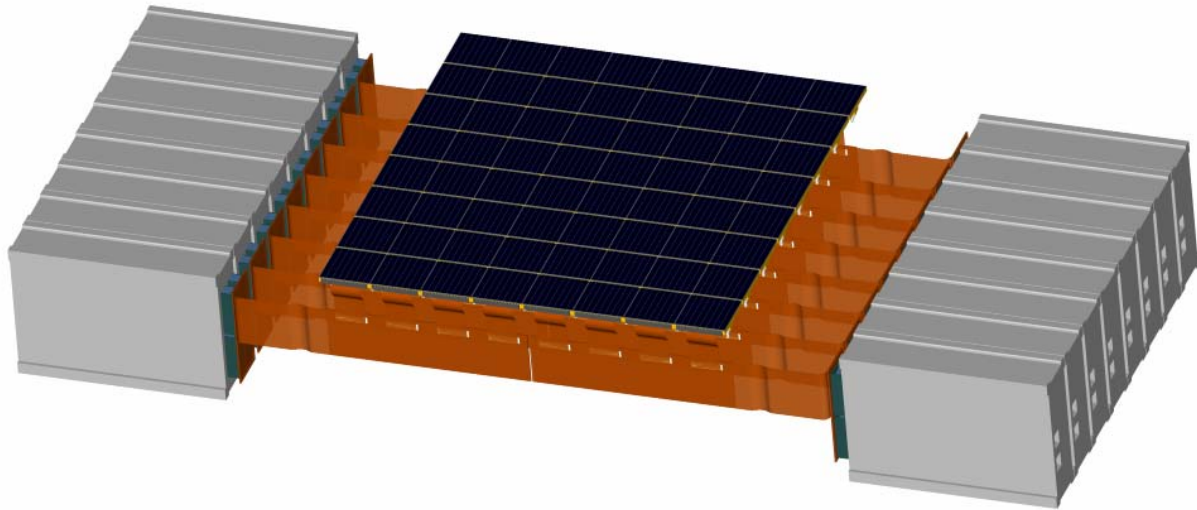
- 100K e- well and expected 4e- noise at 1 MHz
- 2e- noise goal at 100 kHz (guiding)
- ADC bit resolution – approx two bits on the noise
  - $100k / 4 = 25K \times 2 = 50K$  resolution wanted
    - 16 bits = 64K (> 14bits)
- Image memory
  - OTA 4096 x 4096 pixels = 16M pixels = 32MBytes (16 bit resolution)
  - 8 x 8 focal plane = 1Gpixel = 2Gbytes (16bit)
- Data buffering and storage
  - Unless data transport is real time, minimum storage is 2Gbytes, 4Gbytes double buffered.
- Memory access speed minimum ~8 to 16Gbits/sec (1 to 2 Gbytes/sec).
- Full 1Gpixel focal plane readout in ~2sec = ~8Gbits/sec
- Signal processing chain
  - 1Gpixel / 64 OTA = 16Mpixels / OTA
  - 16Mpixels / 8 outputs = 2Mpixels /output
  - 2 sec / 2Mpixels = 954nsec/pixel
  - ADC plus settle time ~1usec per output
  - 1Mhz ADC borderline too slow (unless CDS built-in)
- Controller data transport
  - Maximum speed matches Full 1Gpixel focal plane readout in ~2sec = ~8Gbits/sec
  - Minimum speed equal to shortest expected science integration ~10s = 214 Mbits/sec
- Internal (controller) data path >= 8Gbits/sec
- Path to Pixelserver(s) >= 8Gbits/sec

### Internal Data Throughput Requirements

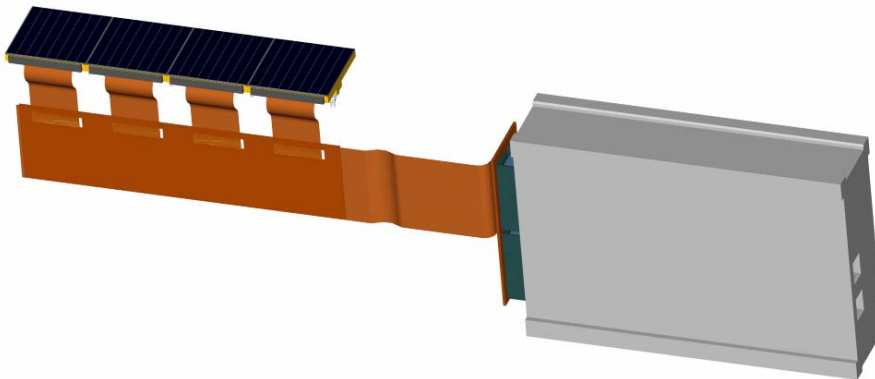
<b>Stage</b>	<b>Array/ADC Readout</b>	<b>1G ethernet</b>	<b>Pixel Processor</b>	<b>Data Storage</b>
<b>Requirement</b>	Goal 128Mbps	Min 64Mbps Goal $\geq$ 256Mbps	Min $\geq$ 256Mbps	Min 64Mbps
<b>Capability</b>	Max 260Mbps (5MSps/ADC x 24)	>800Mbps theoretical	Processor/ memory access (read + write)	Burst ~60Mbps Only ~20MBps sustained
<b>Requirement Notes</b>	33.55 Mpixel/sec (~2sec)		133/400/533Mhz FSB	Duty cycle?

## PHYSICAL FORM FACTOR AND SCALABILTY

The size and shape of the controller electronics is as much of a driver of the design as the electrical requirements. The short cassegrain depth available on the telescope and the size of the focal plane resulted in a horizontal arrangement with the controllers place outboard of the mosaic.



8 x 8 OTA Gigapixel Focal Plane

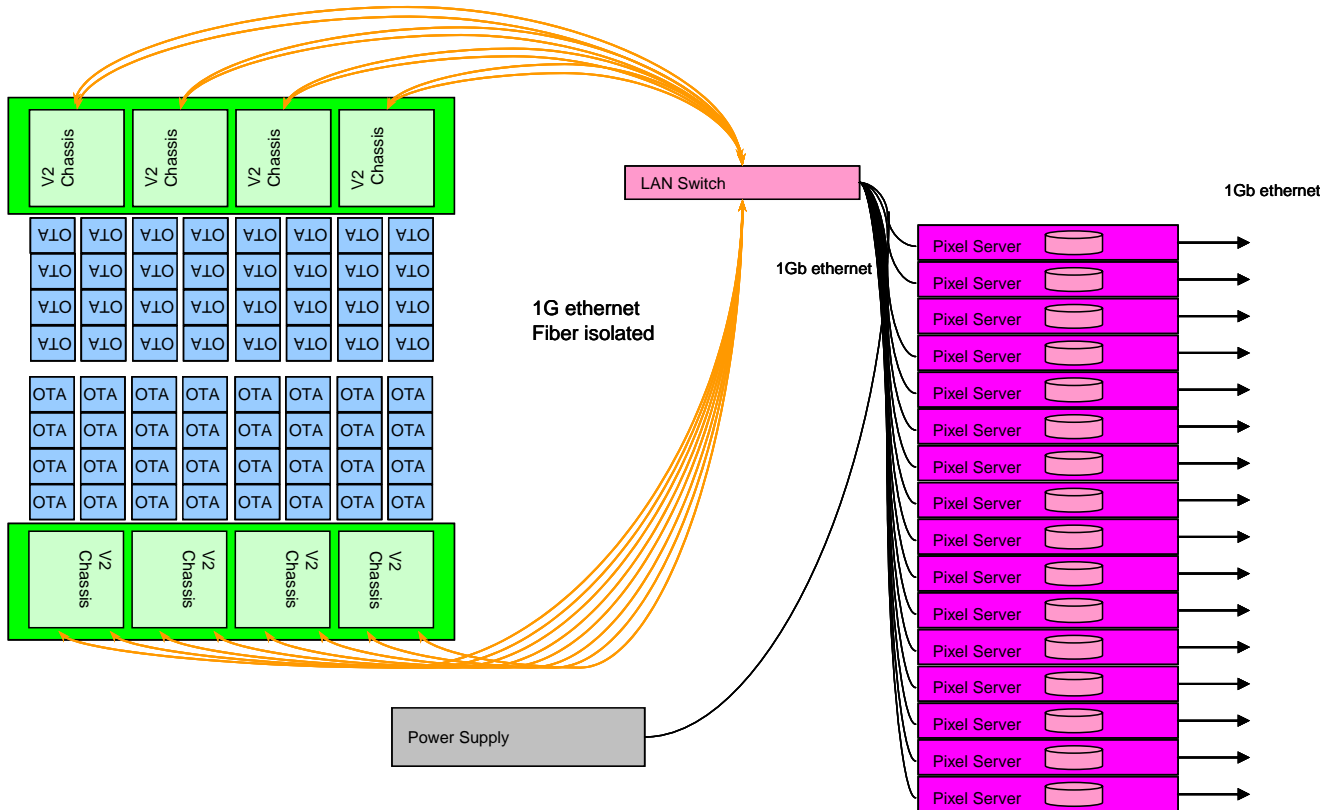


1 x 4 Rigid-Flex Assembly

The 8 by 8 mosaic focal plane was further broken down into 1 by 4 OTA rigid-flex assemblies (see figure). The rigid flex assembly will penetrate the dewar wall and be connectorized for direct attachment to the controller. The ideal size for the chassis would be the width of an individual OTA which is ~50mm. The 3U CompactPCI form factor was chosen due to the availability of off the shelf products including standardized connectors that insure electrical, mechanical, thermal, and EMI performance.

## SYSTEM AND NETWORK ARCHITECTURE

8 STARGRASP chassis will be required for the first Gigapixel camera. Each chassis is an individually removable 4 card slot, fan cooled assembly that controls OTAs. Each card slot is connected via a standard 1 gigabit ethernet fiber link to a commercial network switch which is also connected to a bank of Pixelservers (1U computers). The advantages of this architecture are that there is no custom communications electronics (or associated driver software) required in the Pixelservers, the network is robust, inexpensive and can be reconfigured on the fly.



## PIXELSERVERS AND SOFTWARE PROCESSES

Commercial off the shelf, 1U rackmount server computers have been tested and chosen as the standard Pixelserver platform (although any commercially available equivalent computer type can suffice). The required data storage capacity, communications speed and processing rates meet our requirements (except for the orthogonal guide mode which hasn't been tested yet).

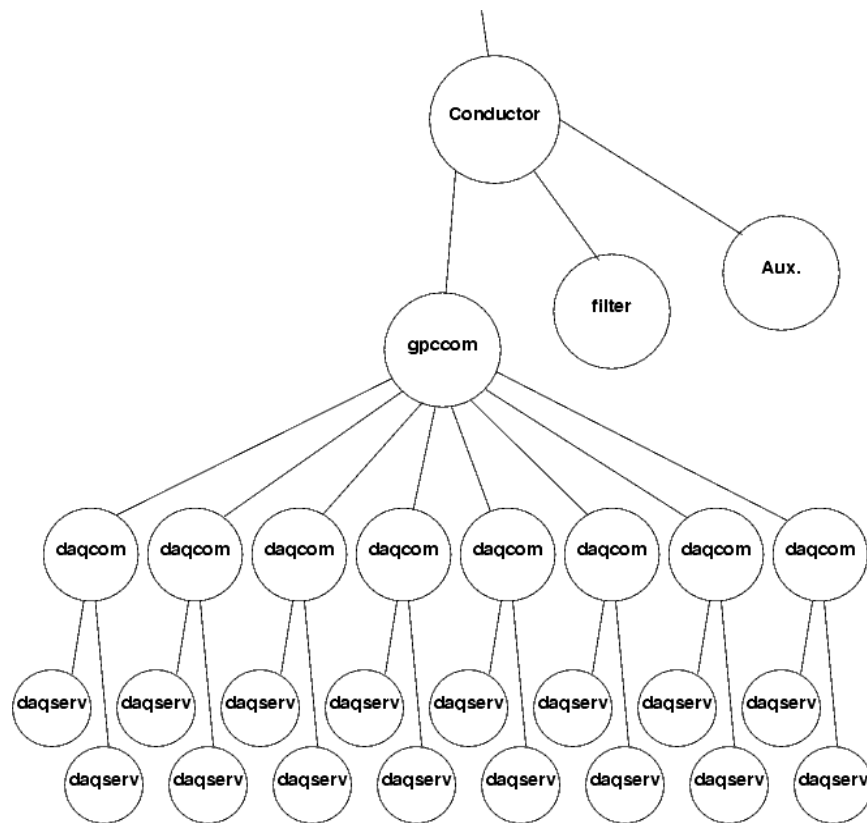
The software running under a LINUX operating system on the Pixelservers consists of several processes.

- Conductor, a combination of scripts, shells, and services providing the glue between gpccom and multiple daqcom processes. Conductor also includes a "status server" which may collect current temperatures, statistics, and user settings from/for gpccom and daqcom.

- Gpccom, Camera client operational software for the camera-level.
- Daqcom , Data acquisition client. Daqcom runs on the pixel server and handles communication with daqserv. It translates an input set of higher level commands into the lower level commands for the embedded system. It also receives UDP pixel data which it combines with header data to form multi-extension FITS format files. Daqcom is built on libraries "libsockio" "libcatp" and "libfh" and "libcli" which are also provided with the package.

On each embedded STARGRASP FPGA, the Daqserv process is running.

- Daqserv, low-level data acquisition server. The software portion of the flash images for the controller FPGA boards. Implements a network service that accepts commands to load parameter sets, select binning and raster sizes, manipulate digital outputs, and trigger readout (TCP/IP socket). Once readout is triggered, pixel data is transmitted by daqserv using UDP/IP to the endpoint specified on the command interface.



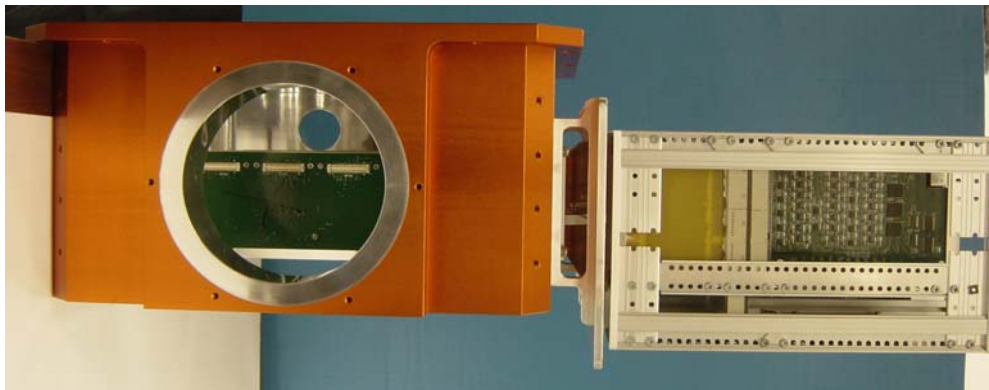
Software Processes

## CRYOGENIC WIRING AND CHASSIS

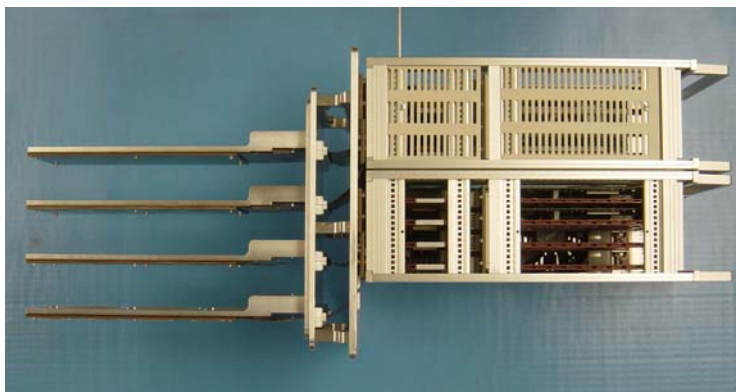
A full Giga pixel camera focal plane has on the order of 4500 OTA signals present in the cryostat. To support this, rigid-flex (combination flex cable and printed circuit board) assemblies were developed. Each assembly connects 4 cryogenically cooled OTAs through the vacuum cryostat wall directly to a backplane with 2mm CompactPCI form factor connectors. The STARGRASP preamplifiers connect directly into these connectors eliminating all hand wiring.



Rigid-flex Assembly



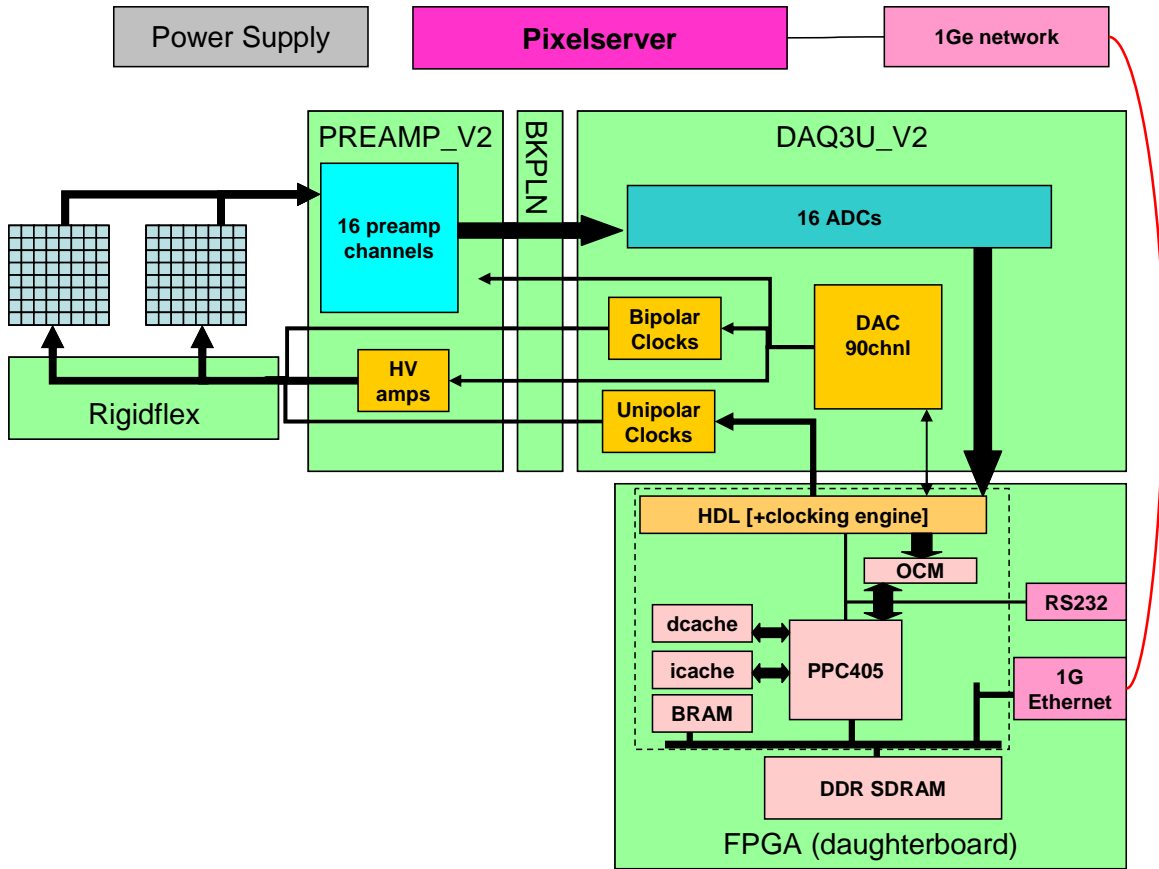
Chassis mounted to cryostat



Dual Chassis mount , top view

### STARGRASP EMBEDDED BOARDSET

A STARGRASP board set consists of a 16 channel (2 OTA) preamplifier, DAQ3U data acquisition motherboard and an FPGA daughterboard.

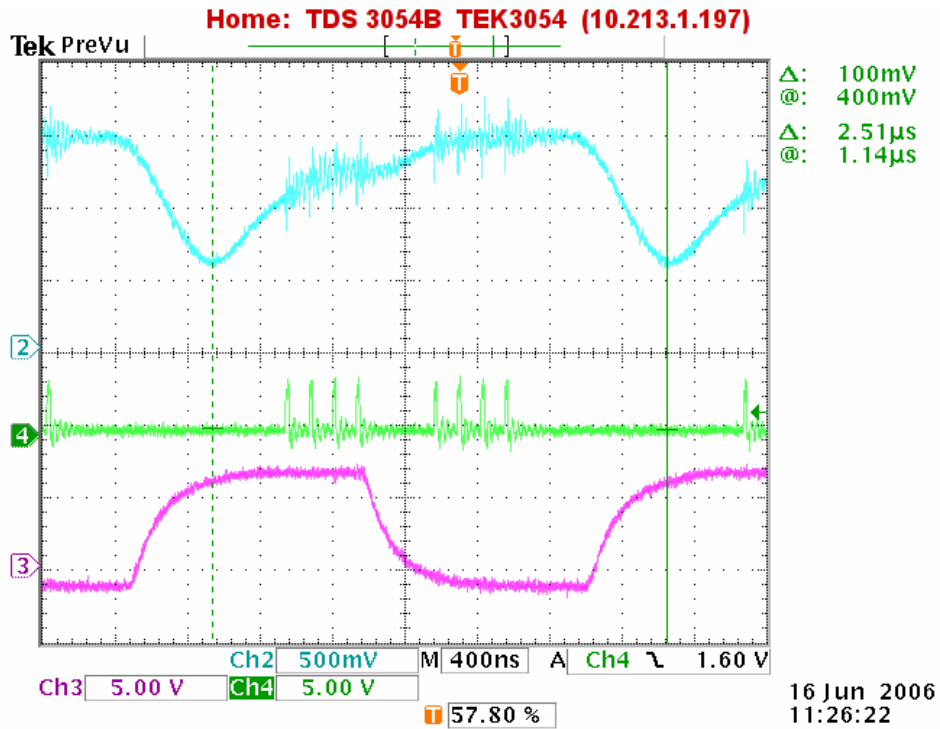


Block diagram

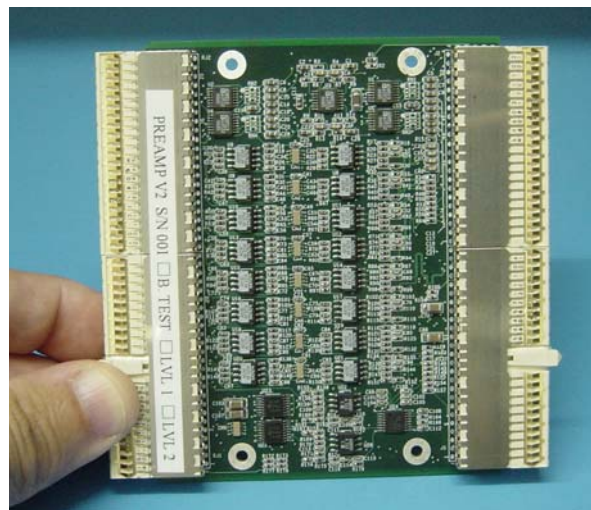
- The Preamplifier board contains 16 channels of OTA amplification, 2 channels of RTD or diode temperature drive and sense, and high voltage buffers. Each amplifier channel has an AC coupled input with a DC clamp function and a 2 pole second stage Bessel filter.
- The DAQ3U board contains 16 individual channels of 10MHz, 3 channel 16bit Analog to Digital Conversion (Analog Devices AD9826). Programmable levels and timing for clocks, biases, and operation of fixed voltage level select signals. The programmable levels are generated by three 32 channel 14bit DACs.
- The FPGA board has a Xilinx Virtex2Pro FPGA which has a hardcore PowerPC CPU running at 300Mhz , a 1 gigbit ethernet fiber interface, and 256MB of DDR ECC SODIMM SDRAM.

### PREAMPLIFIER, MULTIPLE SAMPLING AND DIGITAL CDS

The high ADC conversion speed allows us to apply a multiple sampling scheme on the OTA video signal. As depicted in the oscilloscope trace (video signal in blue on top, sampling time in green and summing well signal on the bottom), high speed multiple samples are taken on both the pedestal and signals levels. The multiple samples can be averaged in the FPGA or farther downstream in the Pixelservers. The Correlated Double Sample calculation is handled digitally in this system and allows the preamplifier to have a simple 2 stage design.



Multiple sampling example



Preamplifier board

## DAQ3U AND ADC COMPONENTS

The proper choice of Analog to Digital Converter (ADC) is critical to achieve the noise, speed and size requirements for the system. After an industry search for an acceptable 16 bit ADC, a series of tests were performed to evaluate the

Analog Devices ADC9826, a 16 bit, ~15 to 12.5MSps, 3 channel 'Imaging Front End'. The AD9826 has several non-ideal specifications including a read noise of 3 LSB and integral non-linearity of 16 LSB<sup>3</sup>. However, the multiple sample averaging technique has been successfully prove to reduce the ADC read noise to 1.69 ADU (Analog to Digital Units)

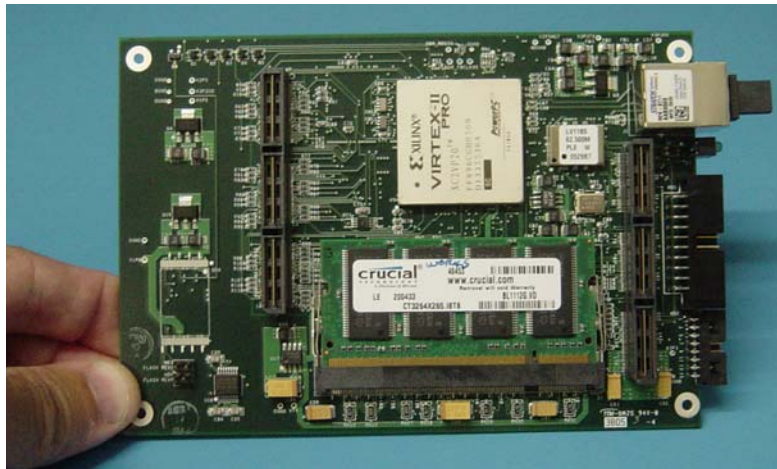
**Table 1 Bench Noise Results**

Test Conditions Single Channel Bench test	300nsec Sample and Hold	100nsec Sample and Hold	100nsec CDS	180nsec CDS with 4 sample digital average
Noise for DC input	3.667 ADU	3.391 ADU	3.546 ADU	1.690 ADU



DAQ3U board

**FPGA BOARD AND EMBEDDED CODE**

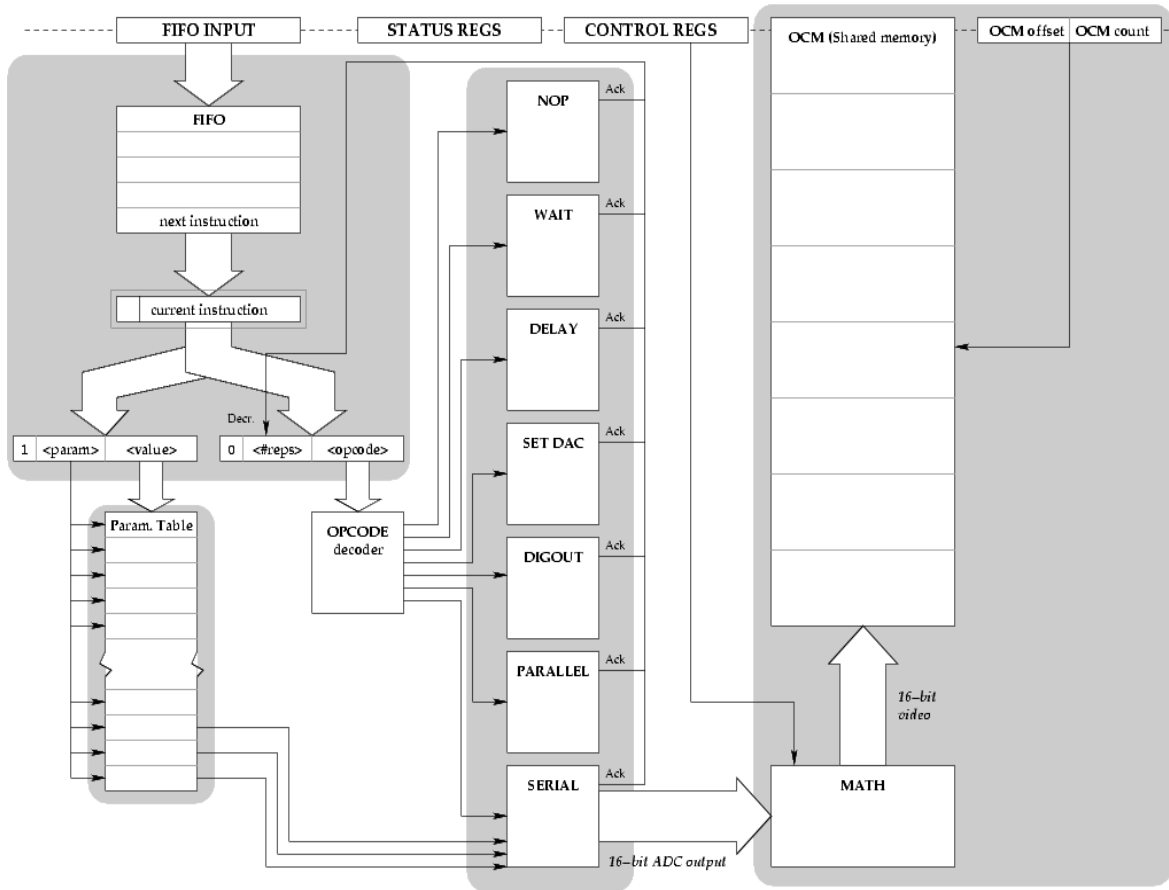


FPGA board

The Virtex2Pro FPGA operates at 2 levels. The PowerPC405 is running a kernel that allows for high speed control and data communication over gigabit ethernet. This level of software also interfaces and controls a lower level of embedded

functionality that provides high speed programmable clocking of the OTAs. This hardware description language based “Clocking Engine” design is a command FIFO structure that executes the following command set:

- Delay for precise amount of time
- Wait for external trigger (sync)
- Set voltages (biases, clock levels)
- Do 1 or more parallel clocking sequence
- Do 1 or more serial+video clocking sequence
- Select cells (by manipulating digital output lines)
- Shift cells during integration (OT correction)
- Provides repeatable, precise timing



Clocking Engine conceptual diagram

A software GUI has been developed to aid in the optimization and test of the different types of Lot#1 and #2 OTAs. Named Cestlavie, it allows an operator to graphically load, edit, save and real time download a CCD clocking pattern to the STARGRASP controller.



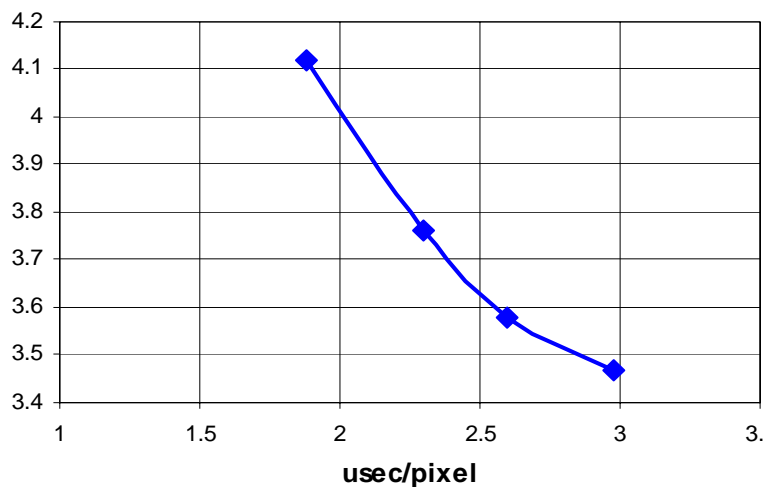
Cestlavie GUI

Data communication throughput across the 1 gigabit ethernet link was been excellent. 400 to 600Mbits per second speeds are achieved with a UDP protocol through commercial network switches. The large SDRAM memory on board makes this possible because it is able to buffer entire device images.

## CURRENT STATUS

Since the Lot#1 OTA devices had higher read noise than hoped for, testing was performed on a low noise CCID20 device. Using a 4 multiple sample readout, we were able to achieve 3 to 4 electron read noise at 1/5 to 3usec per pixel readout rates.

Read Noise at pixel rate CCID20



## CCID20 Read Noise vs Readout rate

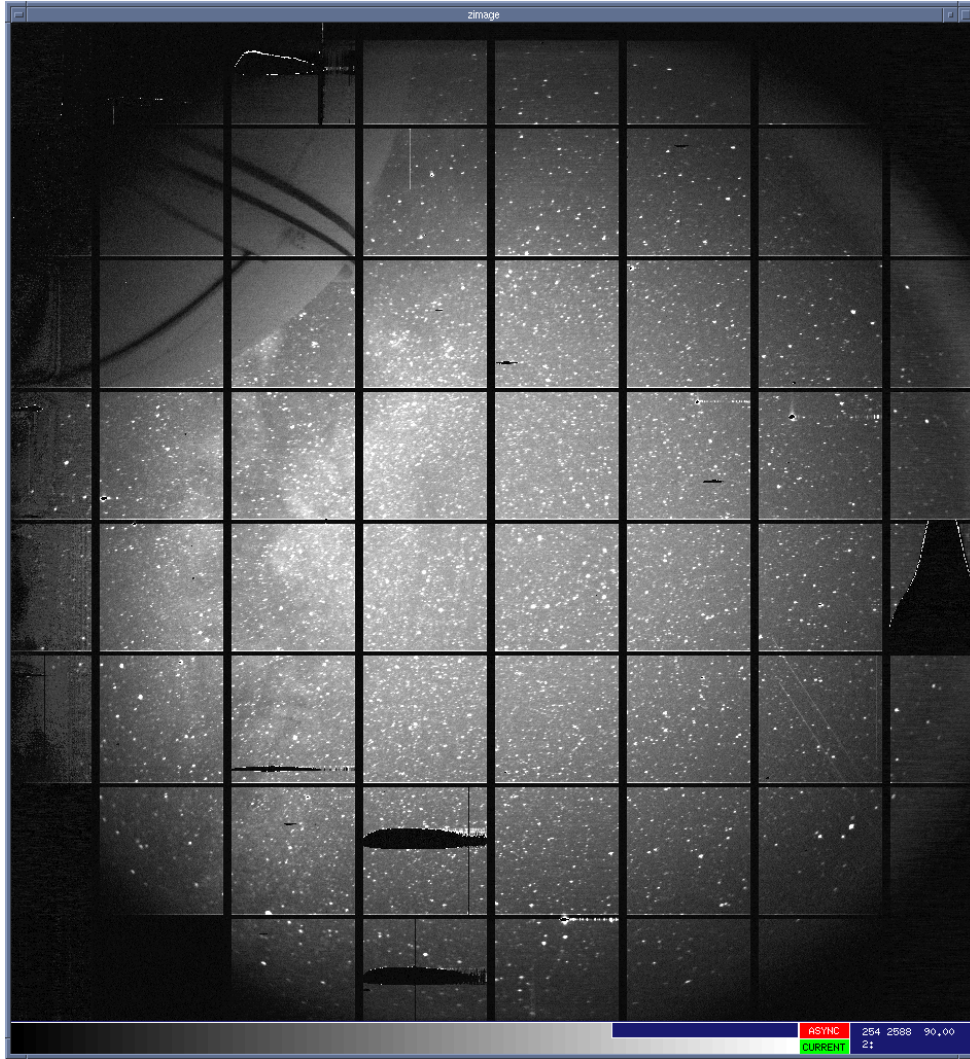
Lot#2 MIT/LL CCID58 OTA testing has just been started and we have verified at least an X2 output gain increase ( $\sim 10\text{uV/e-}$ ) and X2 decrease in read noise ( $\sim 8\text{e-}$  un-optimized operation). Having been thinned to 75micron thickness to increase their red response the Lot#2 devices require a negative bias (5 to -40 volts) on their substrate to achieve good charge diffusion. The improved charge diffusion with substrate bias has been demonstrated and an optimal working voltage is being investigated because a too negative voltage produces bright pixel defects.

The Test Camera #3 which has a 16 OTA focal plane, has been assembled and is undergoing integration and cold tests. It will be the first camera on the PS1 telescope.

A single OTA test camera named Microcam has been assembled on a tripod and on the PS1 telescope. It is being used to evaluate the RFI environment at the telescope site (PS1 is in the near field of several television and radio transmitting towers). The star image was taken outside the dome at the PS1 site..A second Microcam is being planned to help develop the orthogonal transfer correction code for the controller.



Tripod mounted Microcam



Microcam image (outside the PS1 dome)

### ACKNOWLEDGEMENTS

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### REFERENCES

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- <sup>1</sup> Barry Burke et al., elsewhere in these Proceedings.
  - <sup>2</sup> J. Tonry, G. Luppino, N. Kaiser, B. Burke, G. H. Jacoby, "Gig-Pixels and Sky Surveys", in Scientific Detectors for Astronomy, P. Amico, J. W. Beletic, J. A. Beletic, ed., Vol 300, pp. 395-402.
  - <sup>3</sup> Analog Devices AD9826 data sheet, [www.analog.com](http://www.analog.com).